Notice of Allowability	Application No.	Applicant(s)	
	09/701,593	MANZ ET AL.	
	Examiner	Art Unit	
	Albert W Paladini	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/29/00*.

2. ☒ The allowed claim(s) is/are *1-18*.

3. ☒ The drawings filed on *29 November 2000* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Albert W. Paladini 8-17-04
ALBERT W. PALADINI
PRIMARY EXAMINER

Reasons for Allowance

1. The following is an examiner's statement of reasons for allowance: None of the references cited or the art searched disclose or teach alone or in combination the elements and method for simulating and detecting clock circuit behavior including the clocked circuit input using the first code, the synchronous signal method and mechanism, the device and method of marking of the asynchronous signals, the synthesis method and system, the timing and logic method and simulation with the selective deactivation of the test for each insertion of the synchronization module.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Relevant Prior Art

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shrock (5047658) discloses a data synchronizing circuit for synchronizing an input data signal with a clock signal. The synchronizer includes a device for providing a binary product at its device output. This binary product device has a first input, which is connected to the input data signal, and a second input which is connected to the clock signal. The synchronizer also includes a device for providing a binary sum signal at its output. This binary sum device has

a first input, which is connected to the output of the binary product device, and a second input which is connected to its own binary sum output.

Vaidyanathan (5809283) discloses a method of simulating a system which includes components which can simulate a design that includes asynchronous signals, multi-phase clocking, gated clocks, and internally generated state change signals. In one embodiment, each of these signals is treated as a trigger. A trigger causes a change of state in the components (those components that hold state information) of the system. In one embodiment, the analyzer and the elaborator identify the types of processes and the triggers (for those processes that retain state information) in the system. The elaborator determines an order of evaluation of the processes in the system. From the ordered processes, the code generator generates an executable program representation of the system. The run-time system links a process, called a test bench, that drives the triggers (and the data input signals) of the executable program representation of the system.

Graf (6084447) discloses a pulse discriminating clock synchronizer whose function is to provide fast logic generated clock signals for use in CPLDs, FPGAs and other programmable devices to allow higher performance logic derived clock frequencies. It also has a means for synchronizing the logic derived clock signals to the data so as to eliminate the risk of register data signal and clock signal timing mismatches and to eliminate the potential for metastability-induced functional failures. Further, the synchronized logic derived clock signal is produced only when the input logic signal(s) from which the logic derived clock signal is created is (are) recognized as (a) clocking signal(s) (i.e., as opposed to (a) spurious signal(s) or noise).

Smith (6353906) discloses a method of testing synchronization circuitry which includes a simulator sequentially which assigns values to variables and applies simulated signals to elements in the hardware design. More specifically, the simulator steps through a sequence of instructions according to a virtual clock --the simulation time clock. The simulation time clock is a surrogate for an actual hardware clock (or clock input) that will drive the actual circuit. Thus, simulated processes defined as occurring at a first clock or simulation time are executed; giving rise to a first set of simulation results, e.g. signal value changes. Then the simulation time is incremented, and once again the various software processes necessary for modeling operation of the hardware design under simulation are executed, using the results of

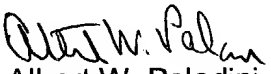
the previous simulation time. As the simulator steps through simulation time in this manner, variable values (modeling physical circuit signals) change and propagate through the circuit.

Akaha (JP407021227A) discloses a logic synthesis method for asynchronous logic circuit where a clock network connected to the clock input of a logic element in the asynchronous circuit is made into a group and detached from the detached from the asynchronous circuit and methodology results in optimization of the asynchronous circuit using a function simulation output.

3. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Albert W. Paladini whose telephone number is (703) 308-2005. The examiner can normally be reached from 7:30 to 3:30 PM on Monday, Tuesday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Leo P. Picard, can be reached on (703) 308-0538. The official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Albert W. Paladini
Primary Examiner
Art Unit 2125

August 13, 2004